

# MC10ELT28, MC100ELT28

## 5 V TTL to Differential PECL and Differential PECL to TTL Translator

### Description

The MC10ELT/100ELT28 is a differential PECL to TTL translator and a TTL to differential PECL translator in a single package. Because PECL (Positive ECL) levels are used, only +5 V and ground are required. The small outline 8-lead package and the dual translation design of the ELT28 makes it ideal for applications which are sending and receiving signals across a backplane.

The 100 Series contains temperature compensation.

### Features

- 3.5 ns Typical PECL to TTL Propagation Delay
- 1.2 ns Typical TTL to PECL Propagation Delay
- PNP TTL Inputs for Minimal Loading
- 24 mA TTL Outputs
- Flow Through Pinouts
- Operating Range  $V_{CC}$  = 4.75 V to 5.25 V with GND = 0 V
- $Q_{TTL}$  Output Will Default High with Inputs Left Open or < 1.3 V
- $Q_{ECL}$  Output Will Default High with Inputs Left Open
- Internal PECL Input Pulldown Resistors
- Pb-Free Packages are Available



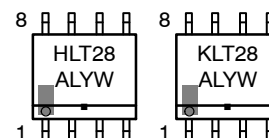
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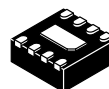
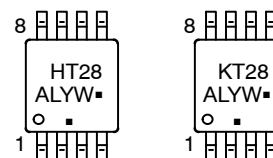
### MARKING DIAGRAMS\*



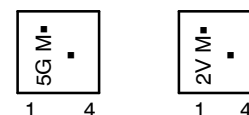
SOIC-8  
D SUFFIX  
CASE 751



TSSOP-8  
DT SUFFIX  
CASE 948R



DFN8  
MN SUFFIX  
CASE 506AA



H = MC10	A = Assembly Location
K = MC100	L = Wafer Lot
5G = MC10	Y = Year
2V = MC100	W = Work Week
M = Date Code	▪ = Pb-Free Package

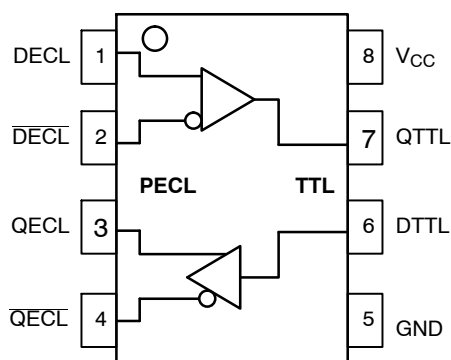
(Note: Microdot may be in either location)

\*For additional marking information, refer to Application Note AND8002/D.

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# MC10ELT28, MC100ELT28



**Figure 1. 8-Lead Pinout (Top View) and Logic Diagram**

**Table 1. PIN DESCRIPTION**

Pin	Function
QTTL	TTL Outputs
DTTL	TTL Data Inputs
QECL, $\overline{QECL}$	PECL Differential Outputs
DECL, $\overline{DECL}$	PECL Differential Inputs
V <sub>CC</sub>	Positive Supply
GND	Ground
EP	(DFN8 only) Thermal exposed pad must be connected to a sufficient thermal conduit. Electrically connect to the most negative supply (GND) or leave unconnected, floating open.

**Table 2. ATTRIBUTES**

Characteristics	Value	
ESD Protection Human Body Model	> 2 kV	
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Pb Pkg	Pb-Free Pkg
	SOIC-8 Level 1	Level 1
	TSSOP-8 Level 1	Level 3
	DFN8 Level 1	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
Transistor Count	71 Devices	
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

1. For additional information, see Application Note AND8003/D.

**Table 3. MAXIMUM RATINGS**

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		7	V
V <sub>IN</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to 6	V
I <sub>out</sub>	PECL Output Current	Continuous Surge		50 100	mA mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	SOIC-8 SOIC-8	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	SOIC-8	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	TSSOP-8 TSSOP-8	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	Standard Board	TSSOP-8	41 to 44 ± 5%	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 lfpm 500 lfpm	DFN8 DFN8	129 84	°C/W °C/W
T <sub>sol</sub>	Wave Solder	Pb Pb-Free	<2 to 3 sec @ 248°C <2 to 3 sec @ 260°C	265 265	°C
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	(Note 2)	DFN8	35 to 40	°C/W

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power)

# MC10ELT28, MC100ELT28

**Table 4. 10ELT SERIES PECL DC CHARACTERISTICS**  $V_{CC}= 5.0\text{ V}$ ;  $GND= 0.0\text{ V}$  (Note 3)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage (Note 4)	3920	4010	4110	4020	4105	4190	4090	4185	4280	mV
$V_{OL}$	Output LOW Voltage (Note 4)	3050	3200	3350	3050	3210	3370	3050	3227	3405	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3770		4110	3870		4190	3940		4280	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3050		3500	3050		3520	3050		3555	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 5)	2.2		5.0	2.2		5.0	2.2		5.0	V
$I_{IH}$	Input HIGH Current			255			175			175	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.3			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.25\text{ V}$ .
- PECL outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $GND$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ .

**Table 5. 100ELT SERIES PECL DC CHARACTERISTICS**  $V_{CC}= 5.0\text{ V}$ ;  $GND= 0.0\text{ V}$  (Note 6)

Symbol	Characteristic	-40°C			25°C			85°C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{OH}$	Output HIGH Voltage (Note 7)	3915	3995	4120	3975	4045	4120	3975	4050	4120	mV
$V_{OL}$	Output LOW Voltage (Note 7)	3170	3305	3445	3190	3295	3380	3190	3295	3380	mV
$V_{IH}$	Input HIGH Voltage (Single-Ended)	3835		4120	3835		4120	3835		4120	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	3190		3525	3190		3525	3190		3525	mV
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 8)	2.2		5.0	2.2		5.0	2.2		5.0	V
$I_{IH}$	Input HIGH Current			255			175			175	$\mu\text{A}$
$I_{IL}$	Input LOW Current	0.5			0.5			0.5			$\mu\text{A}$

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input and output parameters vary 1:1 with  $V_{CC}$ .  $V_{CC}$  can vary  $\pm 0.25\text{ V}$ .
- PECL outputs are terminated through a  $50\ \Omega$  resistor to  $V_{CC} - 2\text{ V}$ .
- $V_{IHCMR}$  min varies 1:1 with  $GND$ ,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ .

**Table 6. TTL OUTPUT DC CHARACTERISTICS**  $V_{CC} = 4.75\text{V}$  to  $5.25\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage	$I_{OH} = -3.0\text{ mA}$	2.4			V
$V_{OL}$	Output LOW Voltage	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{CCH}$	Power Supply Current			27	40	mA
$I_{CCL}$	Power Supply Current			29	42	mA
$I_{OS}$	Output Short Circuit Current		-150		-60	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

## MC10ELT28, MC100ELT28

**Table 7. TTL INPUT DC CHARACTERISTICS**  $V_{CC} = 4.75\text{ V to }5.25\text{ V}$ ;  $T_A = -40^\circ\text{C to }85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$I_{IH}$	Input HIGH Current	$V_{IN} = 2.7\text{ V}$			20	$\mu\text{A}$
$I_{IHH}$	Input HIGH Current	$V_{IN} = 7.0\text{ V}$			100	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$V_{IN} = 0.5\text{ V}$			-0.6	mA
$V_{IK}$	Input Clamp Diode Voltage	$I_{IN} = -18\text{ mA}$			-1.2	V
$V_{IH}$	Input HIGH Voltage		2.0			V
$V_{IL}$	Input LOW Voltage				0.8	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

**Table 8. AC CHARACTERISTICS**  $V_{CC} = 4.75\text{ V to }5.25\text{ V}$  (Note 9)

Symbol	Characteristic	$-40^\circ\text{C}$			$25^\circ\text{C}$			$85^\circ\text{C}$			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Toggle Frequency		TBD			100			TBD		MHz
$t_{PLH}$	Propagation Delay @ 1.5 V DECL to QTTL DTTL to QECL	2.0		5.5	2.0		5.5	2.0		5.5	ns
		0.6		1.2	0.9	1.2	1.5	0.6		1.35	
$t_{PHL}$	Propagation Delay @ 1.5 V DECL to QTTL DTTL to QECL	2.0		5.5	2.0		5.5	2.0		5.5	ns
		0.4		1.0	0.5	0.8	1.1	0.7		1.3	
$t_r, t_f$	Rise/Fall Times (20% – 80%) QECL	0.15		1.5	0.15		1.5	0.15		1.5	ns
$V_{PP}$	PECL Input Swing (Note 10)	200		1000	200		1000	200		1000	mV
$t_r/t_f$	Output Rise Time (10% – 90%) Output Fall Time (10% – 90%)					1.6					ns
						1.1					ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

9.  $R_L = 500\ \Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 2.

10.  $V_{PP}(\text{min})$  is the minimum input swing for which AC parameters are guaranteed.

## MC10ELT28, MC100ELT28

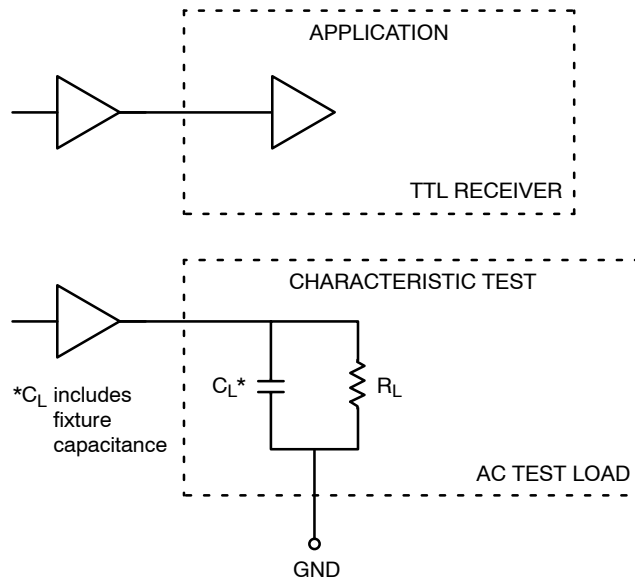


Figure 2. TTL Output Loading Used for Device Evaluation

## MC10ELT28, MC100ELT28

### ORDERING INFORMATION

Device	Package	Shipping†
MC10ELT28D	SOIC-8	98 Units / Rail
MC10ELT28DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC10ELT28DR2	SOIC-8	2500 / Tape & Reel
MC10ELT28DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT28DT	TSSOP-8	100 Units / Rail
MC10ELT28DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC10ELT28DTR2	TSSOP-8	2500 / Tape & Reel
MC10ELT28DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC10ELT28MNR4	DFN8	1000 / Tape & Reel
MC10ELT28MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel
MC100ELT28D	SOIC-8	98 Units / Rail
MC100ELT28DG	SOIC-8 (Pb-Free)	98 Units / Rail
MC100ELT28DR2	SOIC-8	2500 / Tape & Reel
MC100ELT28DR2G	SOIC-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT28DT	TSSOP-8	100 Units / Rail
MC100ELT28DTG	TSSOP-8 (Pb-Free)	100 Units / Rail
MC100ELT28DTR2	TSSOP-8	2500 / Tape & Reel
MC100ELT28DTR2G	TSSOP-8 (Pb-Free)	2500 / Tape & Reel
MC100ELT28MNR4	DFN8	1000 / Tape & Reel
MC100ELT28MNR4G	DFN8 (Pb-Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

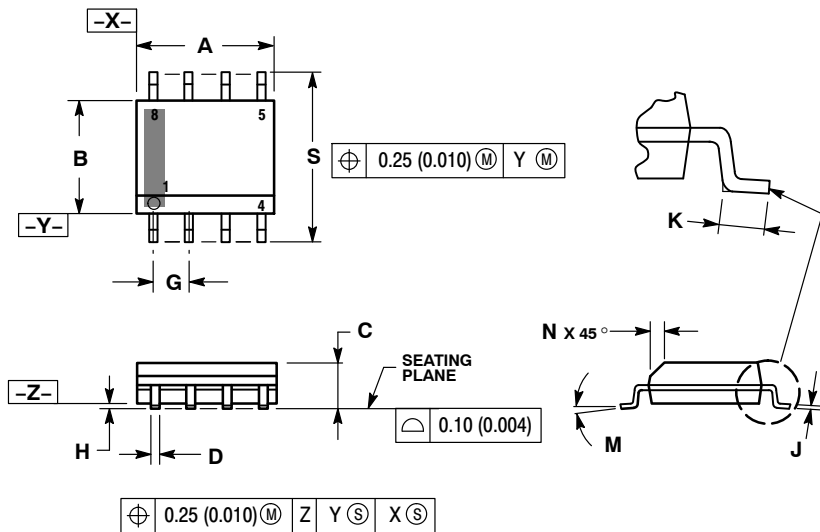
#### Resource Reference of Application Notes

- AN1405/D** – ECL Clock Distribution Techniques
- AN1406/D** – Designing with PECL (ECL at +5.0 V)
- AN1503/D** – ECLinPS™ I/O SPICE Modeling Kit
- AN1504/D** – Metastability and the ECLinPS Family
- AN1568/D** – Interfacing Between LVDS and ECL
- AN1672/D** – The ECL Translator Guide
- AND8001/D** – Odd Number Counters Design
- AND8002/D** – Marking and Date Codes
- AND8020/D** – Termination of ECL Logic Devices
- AND8066/D** – Interfacing with ECLinPS
- AND8090/D** – AC Characteristics of ECL Devices

# MC10ELT28, MC100ELT28

## PACKAGE DIMENSIONS

SOIC-8 NB  
CASE 751-07  
ISSUE AH

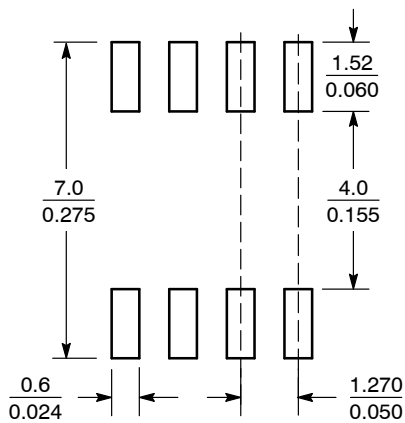


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

### SOLDERING FOOTPRINT\*



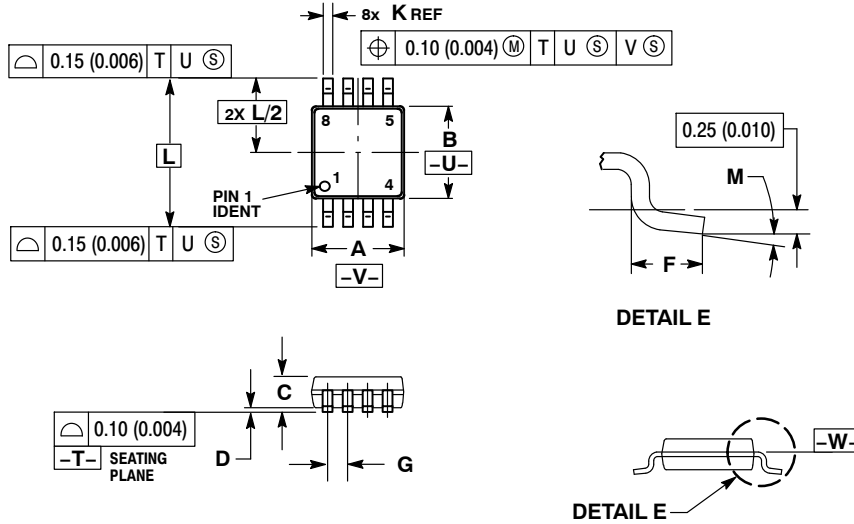
SCALE 6:1 (mm/inches)

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# MC10ELT28, MC100ELT28

## PACKAGE DIMENSIONS

TSSOP-8  
DT SUFFIX  
PLASTIC TSSOP PACKAGE  
CASE 948R-02  
ISSUE A



### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH. PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
6. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

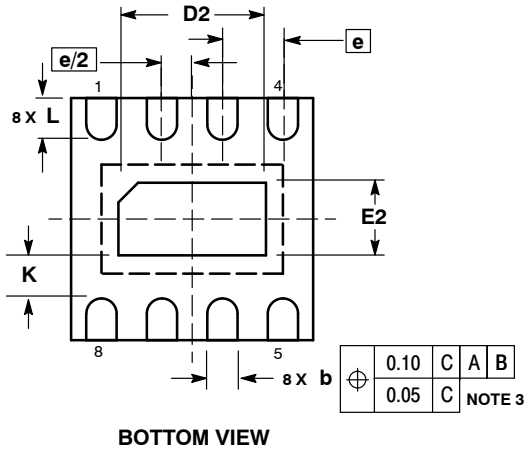
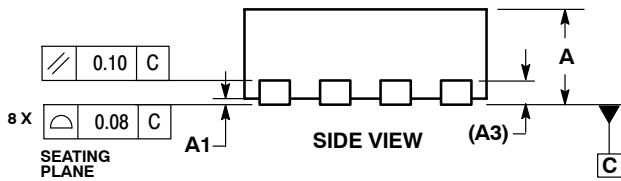
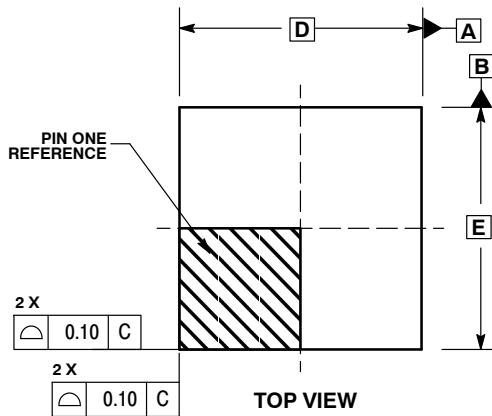
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.80	1.10	0.031	0.043
D	0.05	0.15	0.002	0.006
F	0.40	0.70	0.016	0.028
G	0.65 BSC		0.026 BSC	
K	0.25	0.40	0.010	0.016
L	4.90 BSC		0.193 BSC	
M	0°	6°	0°	6°



# MC10ELT28, MC100ELT28

## PACKAGE DIMENSIONS

DFN8  
CASE 506AA-01  
ISSUE D



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994 .
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.20	0.30
D	2.00	BSC
D2	1.10	1.30
E	2.00	BSC
E2	0.70	0.90
e	0.50	BSC
K	0.20	---
L	0.25	0.35

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